WHAT IS CLAIMED IS:

1. A multiprocessor system, comprising:

a set of processors;

a system board having a set of sockets, each socket suitable for receiving one of the set of processors wherein the number of sockets in the set of sockets exceeds the number of processors in the set of processors;

a set of interconnects providing point-to-point links between at least some of the sockets; and

a pass through device occupying one of the set of sockets, wherein the pass through device connects a first interconnect link connected to the socket and a second interconnect link connected to the socket such that the first and second interconnect links form the functional equivalent of a single interconnect link.

2. The system of claim 1, wherein the system includes a local system memory corresponding to each processor, wherein the local memory of each processor is accessible to each of the other processors.

3. The system of claim 2, wherein the system is characterized by a two tiered memory latency wherein memory accesses to a processor's local memory is characterized by a first memory access latency while memory accesses to the system memory of any other processor are characterized by a second memory access latency.

4. The system of claim 1, wherein the number of sockets in the set of sockets exceeds the number of processors by at least one.

5. The system of claim 1, wherein the point-to-point links consist of power signals, ground signals, and a set of uni-directional data and command signals.

6. The system of claim 5, wherein the point-to-point links are further characterized as HyperTransport links.

7. The system of claim 1, wherein the set of processors include a first processor connected via corresponding instances of the point-to-point link to an I/O bridge, a second processor, and the pass through device.

8. The system of claim 7, wherein the set of processor include a second processor connected via corresponding instances of the point-to-point link to the pass through device and to a third processor.

9. The system of claim 8, wherein the third processor is further connected to the first processor via a corresponding instance of the point-to-point link.

10. A pass through device for use with a data processing system, comprising:

a first set of pins configured to connect to a first set of signals on the system board wherein the first set of signals correspond to a first instance of an inter-chip link;

a second set of pins configured to connect to a second set of signals on the system board wherein the second set of signals correspond to a second instance of the inter-chip link; and

a set of wires connecting the first set of pins directly to the second pins wherein the first instance of the inter-chip link is connected to the second instance of the inter-chip link when the pass through device is inserted in the system board.

11. The pass through device of claim 10, wherein the pass through device comprises an integrated circuit package suitable for insertion into a processor socket of the integrated circuit package.

12. The pass through device of claim 10, wherein the pass through device comprises a printed circuit board suitable for insertion in a processor socket of the system board.

13. The pass through device of claim 10, wherein the first and second inter-chip links comprises first and second instanced of a HyperTransport link.

14. The pass through device of claim 10, wherein the pass through device includes buffering circuitry to boost the strength of the corresponding signals.

15. A data processing system, comprising:

a system board including a set of sockets suitable for receiving a corresponding set of processors and further including a first instance of an inter-chip link connecting a first socket of the set of sockets to a second socket and a second instance of an inter-chip link connecting the second socket to a third socket;

a first processor inserted in the first processor socket;

a second processor inserted in the third processor socket; and

a pass through device inserted in the second socket, wherein the pass through device connects the first instance of the inter-chip link to the second instance of the inter-chip wherein the first processor is directly connected to the second processor via the first and second instances of the inter-chip link.

16. The system of claim 15, wherein each instance of the inter-chip link comprises a point-to-point link.

17. The system of claim 15, wherein the inter-chip link includes a set of uni-directional signals.

18. The system of claim 17, wherein the first and second instances of the inter-chip link comprise first and second instanced of a HyperTransport link.

19. The system of claim 15, wherein the first processor is directly connected to a first system memory and the second processor is directly connected to a second system memory.

20. The system of claim 19, wherein the system exhibits two tiered memory access latency in which access from a processor to its corresponding system memory is characterized by a first access latency and access by any processor to a system memory of any other processor is characterized by a second access latency.

21. The system of claim 15, wherein the system board includes a set of four processor sockets and wherein three of the sockets are populated with processors and the pass through device populates a fourth socket.

22. The system of claim 15, wherein each of the set of processors is enabled to connect to three instances of the inter-chip link.